System And Method For Providing Network Timing Recovery

ABSTRACT

A method and system for network timing recovery that recovers the timing reference by multiplying an 8kHz reference clock up to one of a number of higher frequencies whilst maintaining phase alignment. Further, the present invention allows the 8kHz reference signal to be generated from a software controlled frequency generator where no external reference is available. It also provides a configuration whereby the choice of external or internal 8kHz reference is controlled by software, and further than said 8kHz reference is always used as the input to the phase locked loop (PLL) clock multiplier. An algorithm to control the internal 8kHz generator will not require to take into account "phase jumps" where the frequency suddenly changes by a large amount by passing the generated 8kHz clock through the phase locked loop (PLL), where any large phase increase or decrease on the input clock will be filtered out and not passed though directly to the multiplied clock output.